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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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of

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Complete if Known

Application Number	09/812,030
Filing Date	March 19, 2001
First Named Inventor	Rong Lin
Group Art Unit	Unknown 2124
Examiner Name	Unknown CHAT DO
Attorney Docket Number	87687.042301/R-1265-125

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

Examiner
Signature



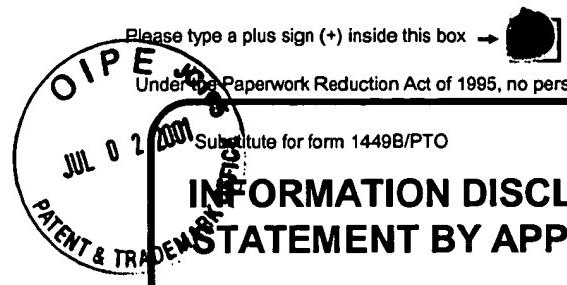
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02/10/04

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¹ Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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Sheet

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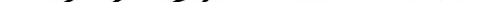
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First Named Inventor	Rong Lin
Group Art Unit	Unknown <i>RIC 4</i>
Examiner Name	Unknown <i>CHAT DO</i>
Attorney Docket Number	87687.042301/R-1265-125

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
CD	1	Lin, Rong, "Parallel Multiplier Designs Utilizing a Non-Binary Logic Scheme", In Proceeding of the First International Symposium on Quality of Electronic Design, San Jose, California, pp. 1-8, (September 2000).	
CD	2	Lin, Rong, "A Reconfigurable Low-Power High-Performance Matrix Multiplier Design", In Proceeding of Euromicro 00, Workshop on Digital System Design, IEEE Press, Maastricht, The Netherlands, pp. 321-328, (September 2000).	

Examiner Signature		Date Considered	2/10/04
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				First Named Inventor	Rong Lin
				Group Art Unit	Unknown - 2124
				Examiner Name	Unknown - Chat Do
Sheet	1	of	2	Attorney Docket Number	
87687.042301/R-1265-125					



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Application Number	TBA
Filing Date	Herewith
First Named Inventor	Rong Lin
Group Art Unit	Unknown K124
Examiner Name	Unknown Chat 1D0

Attorney Docket Number

87687.042301/R-1265-125

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CD	4 5	Lin, Rong, "A Low-Power Regularly Structured Parallel Multiplier Design", Department of Computer Science, SUNY at Geneseo, Geneseo, NY 14454, pp. 1-11, (March 2000).	
CD	5 :	Lin, Rong, "A Reconfigurable Low-Power High-Performance Matrix Multiplier Design", Department of Computer Science, SUNY - Geneseo, Geneseo, NY 14454, pp. 1-11, (March 2000).	
CD	6 -	Lin, Rong, et al, "A Novel Approach for CMOS Parallel Counter Design", Department of Computer Science, SUNY at Geneseo, Geneseo, NY 14454, pp. 1-8, (March 2000).	
CD	7 -	Lin, Rong, "New Circuits for a Regularly Structured Parallel Multiplier Design", Department of Computer Science, SUNY - Geneseo, Geneseo, NY 14454, pp. 1-19, (June 24, 1999).	
CD	8 7	Lin, Rong, "Reconfigurable Buses With Shift Switching -- VLSI Radix Sort", 1992 International Conference on Parallel Processing, CRC Press, Boca Raton, pp. III-2 - III-9, (August 17-21, 1992).	
CD	9 1	Lin, Rong, "Shift Switching and Novel Arithmetic Schemes", IEEE Proceeding of ASILOMAR-29, pp. 580-585, (1996).	
CD	10 :	Ling, Rong, et al., "Reconfigurable Buses With Shift Switching: Concepts nad Applications", IEEE Transactions on Parallel and Distributed Systems, Vol. 6. No. 1. pp. 93-102, (January 1995).	
CD	11 :	Lin, Rong, et al., "Efficient VLSI Architectures for Columnsort", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 7, No. 1, pp. 135-139, (March 1999).	

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